## REMARKS

In paragraph 1 of the office action, the examiner objects to drawings Fig. 1 for containing misspelling of Successful; Fig. 2 and Fig. 3 for not including textual labels. The applicant has amended the drawings accordingly. The applicant respectfully submits that the drawings as amended put the application in condition for allowance, which allowance is respectfully requested.

The applicant has canceled claims 2-7 and 10-57 and added new claims 58-93. The applicant submits the amended claims are allowable, which allowance is respectfully requested.

In paragraph 3 of the office action, the examiner rejects claims 1-57 under 35 USC 103(a) as being unpatentable over US Patent No. 6,181,159 to Rangasayee.

Rangasayee is directed to a matrix switch for programmably routing communications signals to a plurality of I/O ports of the switch. Rangasayee is silent on assigning "a special number and type of interfaces to each I/O device" according to the present invention as shown in claim 1. Rangasayee has only ports of uniform design and provides paths between ports.

Rangasayee is further silent on "assigning I/O pins according to the needs of each I/O device" according to the present as shown in claim 8. Rangasayee has only uniform ports having fixed I/O pins per port and does not contemplate adjusting the pins of each port according to the protocol needed by the device.

Rangasayee is silent on "switching in hardware using ID bits on each I/O device" according to the present as shown in claim 9.

The present invention receives ID bits (I/O device value) and, based on the ID bits, assigns I/O pins and interface protocol of the controller to communicate with attached devices.

In paragraph 4, the examiner states that "Rangasayee does not disclose expressly the I/O devices are initialized or the step of performing the assignments of special number and type of interfaces during initialization. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to initialize the programmable switch matrix device such that the special routing pathways to connect the various I/O devices are established before communications begins. The suggestion/motivation for doing so would have been programmable devices, in particularly CPLDs and FPGAs require initial instruction on how to configure the logic blocks and programmable routs on the device prior to ordinary use. This step is always done during initialization where an external source sends configuration data to the programmable device in order to configure the device for the desired functionality as is well known to one of ordinary skill in the art. Therefore, it would have been obvious to initialize the programmable logic device according to the specification of the I/O devices, e.g., the desired routing configuration, prior to actual use." The applicant disagrees. The applicant respectfully submits that the elements are not common knowledge and requests the examiner provide adequate evidence according to MPEP 2144.03C as well as motivation to combine. Neither the art cited, nor the examiners claimed common knowledge would result in the present invention.

In fact, Rangasayee teaches away from the invention by providing only a port router. There is no controller function within Rangasayee. Therefore, a controller for communicating with a plurality of I/O devices is not contemplated by Rangasayee. With Rangasayee, one could connect a controller to a port and devices to other ports of the matrix but the controller would not configure any I/O signals or protocols of the present invention. Rangasayee would result in a controller for each protocol and

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each port would have I/O pins for a single device having the maximum pins contemplated for i/o devices. The present invention permits a single controller to communicate to i/o devices through interfaces customized for protocol and signal pin function based on an ID field.

Therefore the applicant submits that claim 1 is allowable, which allowance is respectfully requested.

In paragraph 7, the examiner says "As per claims 8-21, Rangasayee discloses claim 1 wherein switch matrix is configurable to the needs of the various devices attached to it (Fig. 11 shows routing is performed based on which devices needs to communicate with another device), the configuration data generated by the microprocessor (Col 9, lines 1-12) or prom (FPGAS initialized generally with PROM data) dictating which virtual circuit to create". The applicant disagrees. The present invention "assigns I/O pins according to the needs of each I/O device". Rangasayee only routs signals to device via ports having fixed I/O. Rangasayee does not contemplate assigning I/O pins according to the requirements of individual devices.

Therefore the applicant submits that claim 8 is allowable, which allowance is respectfully requested.

Rangasayee is also silent on switching in hardware using ID bits on each I/O device as shown in claim 9. The present invention provides ID bits to indicate to the controller the protocol and I/O configuration required by an attached device. Rangasayee only routs signals between ports having fixed I/O configuration.

Therefore the applicant submits that claim 9 is allowable, which allowance is respectfully requested.

New claim 58-93 are allowable as they comprise the novel elements of a self configuring controller for configuring I/O signal pins and communication protocol based in an ID value related to I/O devices attached to the controller.

Therefore the applicant submits that claims I, 8-9, and 58-93 are allowable, which allowance is respectfully requested.

It is respectfully submitted that the application is now in condition for allowance, which allowance is respectfully requested.

RESPECTFULLY SUBMITTED

JOHN E. CAMPBELL-AGENT

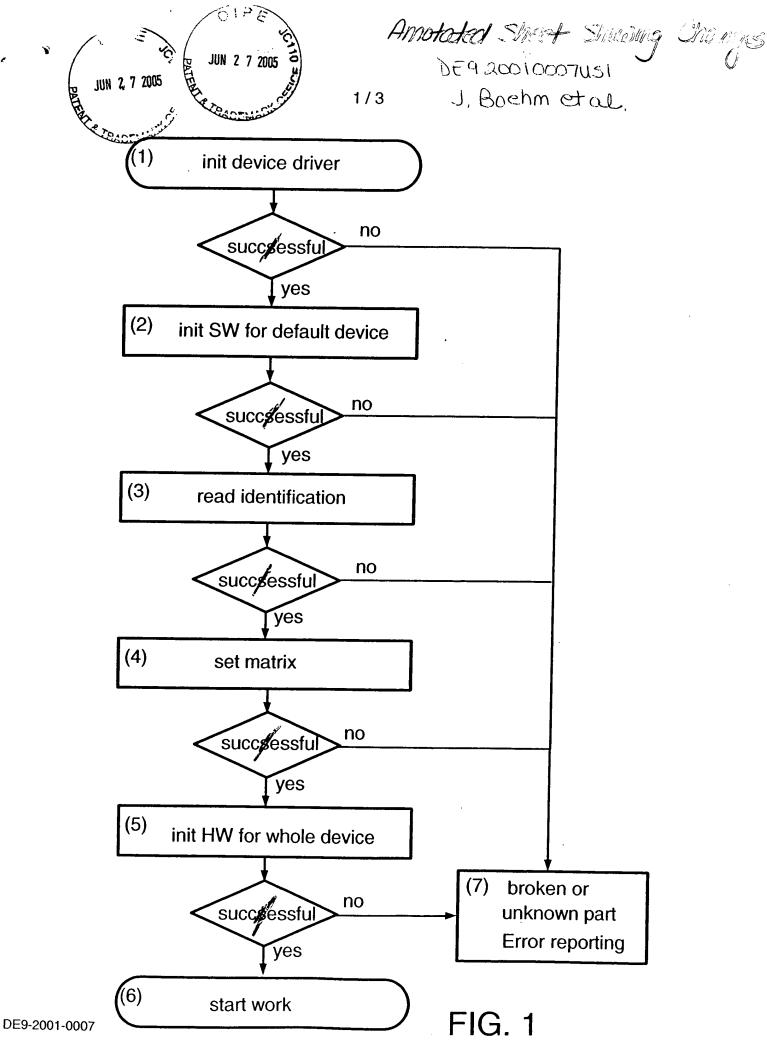
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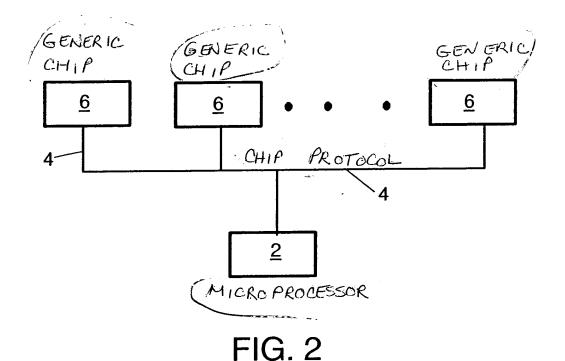
## **Amendments to the Drawings:**

The attached sheets of drawings include changes to FIGs. 1-4. In FIG. 1 spelling of successful has been corrected. In FIG. 2 textual labels have been added. In FIG. 3 textual labels have been added. I FIG. 4, textual labels have been added and the drawing allegiance of reference number 6 has been corrected.

Replacement sheets and annotated sheets are attached hereto.



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GENERIC GENERIC, GENERIC CHIP CHIP CHIP <u>6</u> <u>6</u> <u>6</u> Controller CONTROLLER CONTROLLER NETWORK INTER FACE 12 12 -12 MAIN/

FIG. 3

